

FIG. 1 is a block diagram of a functional circuit testing system. The system includes an external tester (ET) connected to a functional circuit (FC) via signal line S1. The functional circuit is connected to an S-tester (ST) via signal line S3. The S-tester is connected to a logic circuit (LM) via signal line S2. The logic circuit outputs FOUT to the functional circuit and receives FIN from the S-tester. The functional circuit outputs FS to the S-tester. The entire system is labeled 1.

The diagram illustrates the S-Tester system architecture. It shows a sequence of components: an input signal **FIN** enters a processing unit (represented by a large rectangle). Inside this unit, the signal passes through a series of blocks labeled **L**, **SP**, **FF**, and **L** again. The signal then passes through two circular components labeled **TP**. The output of the processing unit is **FOUT**. Below the processing unit, there are three vertical lines representing signals: **SPIN**, **TPIN**, and **TPOUT**. These signals are connected to a block labeled **ST** (S-Tester). The **TPIN** and **TPOUT** signals are also connected to the **TP** components within the processing unit.

FIG 3

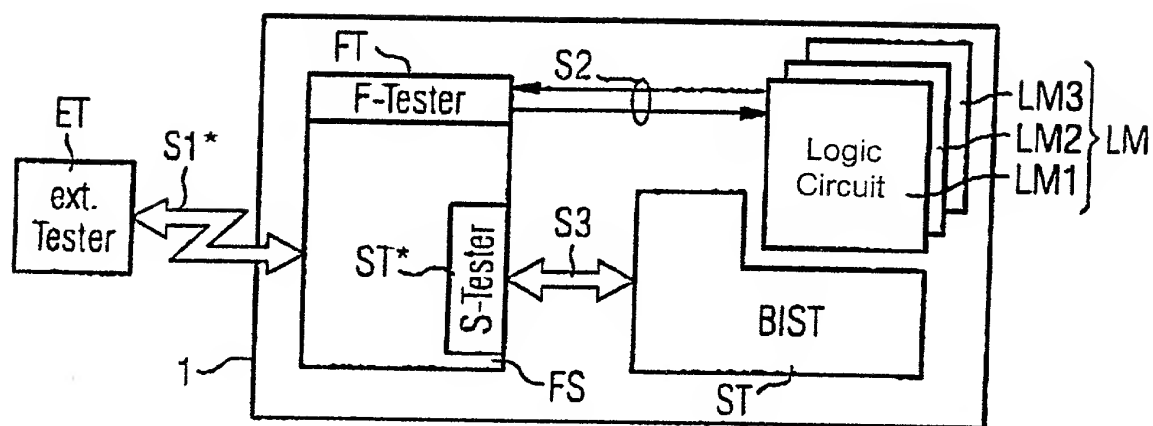


FIG 4

PRIOR ART

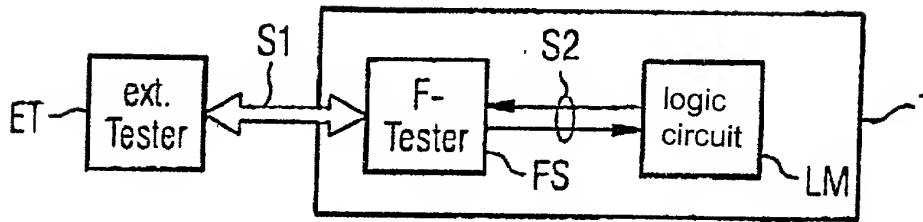


FIG 5

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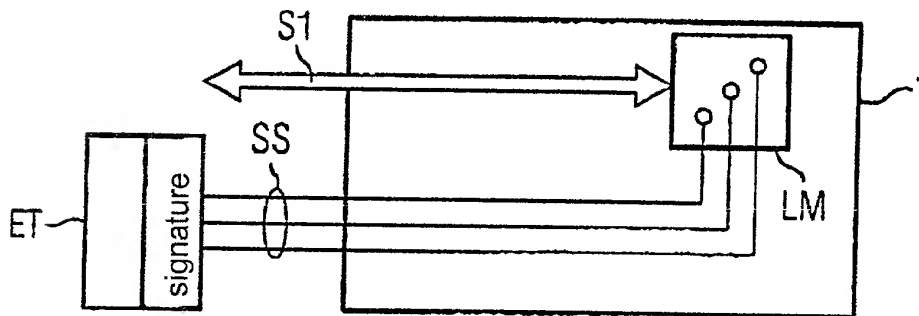


FIG 6

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